IN THE SPECIFICATION:

Please add the following new paragraph after the Title on page 1:

--The present patent application is a continuation of co-pending United States Patent Application Serial No. 10/225,514 filed August 21, 2002, which in turn is a continuation of United States Patent Application Serial No. 09/730,937 filed December 6, 2000, now United States Patent No. 6,489,592, which in turn is a continuation of United States Patent Application Serial No. 09/336,804 filed June 21, 1999, now United States Patent No. 6,207,929.--

Please replace the paragraph beginning at page 10, line 3 with the following new paragraph:

--Referring now to dedicated power supply PS1. This power supply, in the preferred embodiment, includes an inverter stage 40 including a high frequency switching type inverter 42 provided with power from three phase voltage source 44 having a frequency of 50 or 60 Hz according to the local line frequency. The AC input voltage is rectified by rectifier 46 to provide a DC link 48 directed to the input of inverter 42, which is operated at a high frequency in excess of 18 kHz. The output or load of inverter 42 is transformer 50 having primary winding 52 and secondary winding 54 with a grounded center tap 56 connected to ground 58. High frequency pulses at the input of transformer 50 are drastically higher than line frequency at voltage input 44 to reduce the size of the components necessary for the inverter. Secondary winding 54 is directed to rectifier circuit 60 having diodes D1, D2, D3 and D4 to create a positive output terminal 62 and a negative output terminal 64 connected to the output switching network 70. The switching network operates at a low frequency of less than 200-300 Hz. Output switching network 70 includes two transistor type switches SW1 and SW2, usually in the form of IGBT's that can be turned on and off according to the logic on base lines 116, 118. To dissipate high voltages when switches SW1, SW2 are off, snubber networks 100, 102 are connected across the switches. Network 70 is used for pulsating high welding currents substantially over 200 amperes. A single output inductor 110 is divided into positive pulse section 112 and negative pulse section 114. In this manner, an AC current is created

in output lines 120, 122 connected to electrode 12 and grounded plates 20, 22. Power supply PS2, shown in the bottom portion of FIGURE 2, has output line 120 connected to tandem electrode 14 and output line 122 also connected to the grounded base plates 20, 22. By alternating the logic on base control lines ~~126, 128~~ 116, 118 in succession, an alternating current is applied to the welding circuit of the individual tandem mounted electrodes. Inverter 42 is controlled by microprocessor controller 200, which controller is somewhat standard. It has an output to control pulse width modulator 202, driven by oscillator 204. The oscillator in practice has a frequency exceeding 18 kHz and preferably has a frequency in the range of 20-40 kHz. Consequently, the switching inverter 42 operates at a high frequency in excess of 20 kHz to convert the three phase input voltage at source 44 into a high frequency current output at primary winding 52 of transformer 50. The pulse width modulator is operated at the frequency of oscillator 204 by pulses on control line 206. The duty cycle of the individual pulses controls the amount of current being created by inverter 42 and is determined by the voltage on input line 210 which is the output of error amplifier ~~214~~ 212 generating a voltage according to the difference between a voltage representing actual arc current from shunt 220 by way of line 222. Feedback circuit 224 applies a voltage on input 226 that represents the instantaneous arc current or voltage. A second input 230 is the wave shaping output signal from controller 200. The relationship between input 226 and input 230 at error amplifier 212 determines the voltage on line 210 and, thus, the duty cycle at any given time for pulse width modulator 202. This control circuit is standard architecture for a switching type inverter so the current being transmitted by inverter 42 is controlled in accordance with the output signal on line 230 of controller 200.--

Please replace the paragraph beginning at page 11, line 22 with the following new paragraph:

--Referring now to FIGURE 3, the control for power supplies PS1 and PS2 are illustrated as hardwired flip-flops 240 and 240a, respectively. Details of flip-flop 240 will be described. This description applies equally to flip-flop 240a, wherein the elements have the same number, but are

designated with the subscript a. Flip-flop 240 is a software program to produce alternating logic in base control lines 116, 118 at a desired frequency. Flip-flop 240 controls the alternate switching of switches SW1 and SW2 at a low frequency to produce a low frequency output for network 70 as shown in FIGURE 2. The logic in lines 116, 118 is the output of non-coincident terminals 242, 244 of flip-flop 240. The logic on these terminals is alternated according to the logic at either the set terminal 246 or the reset terminal 248. To change the logic on lines 116, 118 the logic on terminals 246, 248 are reversed at a frequency determined by the control circuit 250 in the form of a software voltage frequency oscillator 252 having an output frequency determined by the setting or adjusted voltage of control circuit 254 for frequency f_1. This is the low frequency for alternating the logic on lines 116, 118. This is the frequency of the welding current at electrode 12. The output of the voltage control oscillator 252 is the logic on line ~~156~~ 256 connected to set terminal 246 and through inverter 258 to reset terminal 248. A positive pulse at the output of oscillator 252 sets flip-flop 240 to create a logic 1 in line 116. A logic 0 at the output of oscillator 252 has the reverse effect and creates a logic 1 at terminal 248 and, thus, a logic 1 at the inverted output terminal 244 to produce a logic 1 in line 118. A logic 1 in line 116 or line 118 turns on the switch SW1 or SW2. When the logic 1 shifts to the opposite output line, the transistor type switch shifting to a base at logic 0 immediately turns off. Thus, by adjusting the output of circuit 254, frequency f_1 of network 70 in PS1 is determined. In a like manner, adjusting the frequency by changing circuit 254a produces a desired frequency f_2 for consumable electrode 14. In accordance with the invention, a software program or other standard electrical architecture is used to control the frequency f_1 and f_2 of the current of the welding operation for electrode 12 and electrode 14. These frequencies are controlled separately to prevent arc interference. The operation of the invention as illustrated in FIGURE 3 is shown in FIGURE 4 wherein the frequency f_1 of electrode 12 is a low frequency, but substantially greater than the frequency f_2 for electrode 14. Frequencies f_1 and f_2 have no relationship to the input line frequency of voltage source 44 and no relationship to the high frequency of inverter 42. Consequently, the present invention involves a tandem electrode welder wherein the output network

creates a given low frequency for each of the tandem electrodes. The frequencies are independently controlled and have no relationship with each other. This welder is an advance in the art and is advantageous in high current welding which arc noise must be suppressed.--

Please replace the paragraph beginning at page 16, line 1 with the following rewritten paragraph:

--To provide a simplified phase shift implementation of the present invention, system 300 illustrated in FIGURE 9 has been devised. Electrode 12 and 14 conduct alternating welding current from power supplies ~~310, 312,~~ 311, 313 respectively. Power supply ~~310~~ 311 include high frequency inverter PS_A with a three phase input 320 and output terminals 322, 324. A pulse width modulator 330 causes the shape of the current pulses to be controlled by error amplifier 332 with a pulse shape input 334 from master controller MC. Arc current sensed from shunt 340 as voltage signal I_{a1} is forced to follow the shape of the voltage signal from master controller MC on line 334. Switching network ~~350~~ 351 is like network 70 shown in FIGURE 2. The network alternates as the logic on lines ~~352, 354~~ 353, 355 is alternated by flip-flop A. The frequency of the welding current at electrode 12 is controlled by the frequency of changes in synchronizing line ~~360~~ 361 through non-inverted input ~~362~~ 363 and the inverted input 364 at terminals S, R, respectively. In a like manner, the frequency of the weld current at electrode 14 is controlled by the non-inverted input 400 and inverted input 402 of power supply ~~312~~ 313. Other components of this second power supply are the same as the like components of power supply ~~310~~ 311 and are numbered accordingly, except for pulse shape input 404 from master controller MC. The signal in line ~~360~~ 361 is delayed slightly by delay circuit 410 to produce a phase shift between the AC welding currents of electrodes 12, 14. The delay is substantial less than ½ period of the frequency on synchronization line ~~360~~ 361. If 60 Hz is used, delay is less than 5-6 ms.--

Please replace the paragraph beginning at page 16, line 18 with the following rewritten

paragraph:

--In operation, system ~~300~~ 301 has an AC synchronizing signal in line ~~360~~ 361 with alternating positive commands and negative commands. In the illustrated embodiment, a positive command is a logic 1. The negative command is a logic 0. When the synchronizing signal on line ~~360~~ 361 is a logic 1, a positive current pulse is caused by a logic 1 on line ~~352~~ 353 and a logic 0 on line ~~354~~ 355. When this positive command is created, delay circuit 410 delays a logic 1 on line ~~352~~ 353 to flip-flop B. Thus, the weld current are out of phase by the delay of circuit 410. The low frequency of less than about 300 Hz is the same for both electrode 12, 14. Consequently, a simplified phase shift is provided using power supplies with the output switching networks shown in FIGURE 2. If there are more than two electrodes, a further delay circuit 420 or up to N delays represent by delay 422 can be used.--

Please replace the paragraph beginning at page 16, line 27 with the following rewritten paragraph:

--In accordance with the invention, the positive going command in synchronization line ~~360~~ 361 can force the power supplies into a positive pulse. Thereafter this weld current will oscillate until a negative command forces the pulse into a negative pulse. By this concept used in an implementation of the invention, the frequency of the weld currents is higher than the frequency of the synchronization signal while maintaining a forced phase shift. Such a system is shown in FIGURE 10 where the output of delay circuit 410 is a delayed synchronization signal. When the delayed signal shifts positive, i.e. to a logic 1 in line 412, pulse generator 450 starts operation at frequency f_{10} with a forced first positive pulse. The next logic 1 in line 412 restarts the pulse generator with a forced positive pulse. These forced positive pulses are out of phase with similar forced pulses at flip-flop A by the delay of circuit 410. Consequently, the modification of system ~~300~~ 301 as shown in FIGURE 10 gives out of phase welding currents with frequencies determined at the individual power supplies, which frequencies are different. In the system of FIGURE 10 without a

pulse generator at the input of flip-flop A, flip-flop B is out of phase and frequency f_{10} at flip-flop B is greater than the frequency of the synchronization signal operating flip-flop A.–